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CAD for VLSI Design . SPRING 2014-15 . Course Outline: Introduction: VLSI design flow, challenges. Verilog /VHDL: introduction and use in synthesis, modeling combinational and sequential logic,

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writing test benches.. Logic synthesis: two-level and multilevel gate-level optimization tools, state assignment of finite state machines.

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ELEC 5250/6250/6256 - Computer-Aided Design of Digital Circuits Fall Semester, 2018 Instructor: Victor P. Nelson, Professor of ECE Syllabus: ELEC 5250/6250/6256 Important Dates: · Labor Day Holiday: Monday, September 3 · Midterm Exam (date TBA) · Fall Break: Thursday-Friday, October 11-12 · Thanksgiving Holidays: Monday-Friday, November 19-23

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Author's Guide

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